REMARKS/ARGUMENTS

No claims are amended, canceled, or added by this response. Accordingly, claims 1 and 5-9 remain pending.

Embodiments in accordance with the present invention relate to semiconductor packages featuring a diepad having a supplemental downbond portion to receive a bond wire. As shown in Figures 5 and 6 of the instant application that are excerpted below, this configuration enhances the efficiency of utilization of available space by the package:

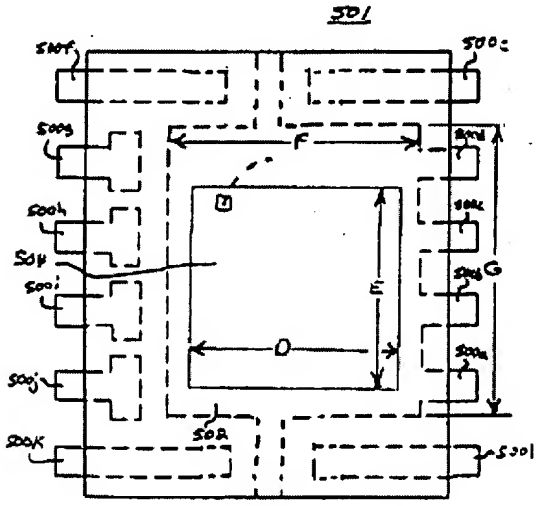


FIG. 5
(Prior Art)

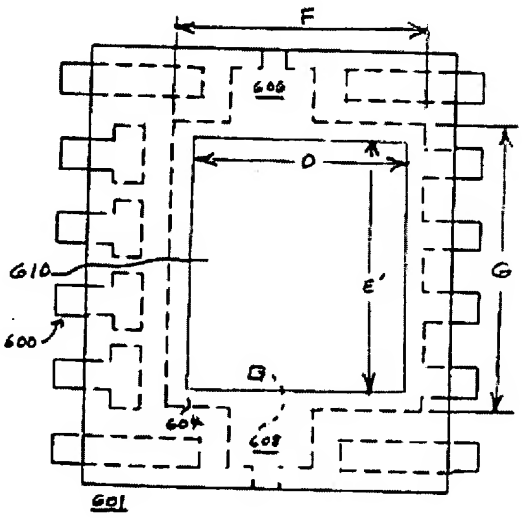


FIG. 6

[0054] Fig. 6 shows a corresponding twelve lead package 601 in accordance with an alternative embodiment of the present invention. Lead frame 600 of package 601 features diepad 604 having two supplemental downbond portions 606 and 608 positioned at either end of the package. In the package shown in Fig. 6, PIC die 610 having a length E' of 2.073 mm and a width D' of 1.47 mm (die area 3.047 mm^2) is housed on a diepad 604 having the same dimensions as that of Fig. 5, resulting in an improved space efficiency of 84.5%. (Emphasis added; ¶**[0054]**)

Sole pending independent claim 1 recites as follows:

1. A package for a semiconductor device comprising:

a semiconductor die having a laterally conducting structure and a ground contact on an upper surface; and

a leadframe comprising,

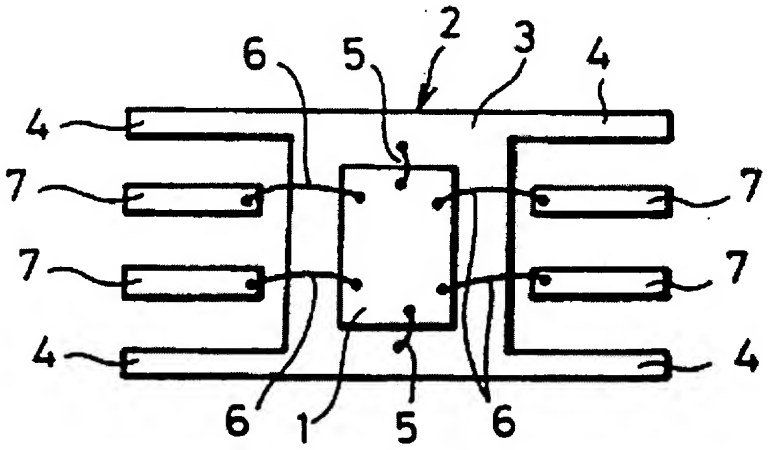
a diepad in contact with a lower surface of the die,
a lead separated from the diepad, and
a supplemental downbond diepad portion projecting from a main portion of the diepad and configured to receive a downbond wire from the ground contact, the supplemental diepad portion positioned between an end of the package and the die, and immediately between the lead and a second lead that is also separate from the diepad. (Emphasis added)

Independent claim 1 stands rejected as anticipated by U.S. patent no. 5,057,805 to Kadowaki et al. ("the Kadowaki patent"). This anticipation rejection is traversed as follows.

As a threshold matter, the Examiner is respectfully reminded:

for anticipation under 35 U.S.C. 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. (Emphasis added; MPEP 706.02)

In rejecting the claims as anticipated in the most recent office action, the Examiner relied heavily on Figure 2 of the Kadowaki Patent:

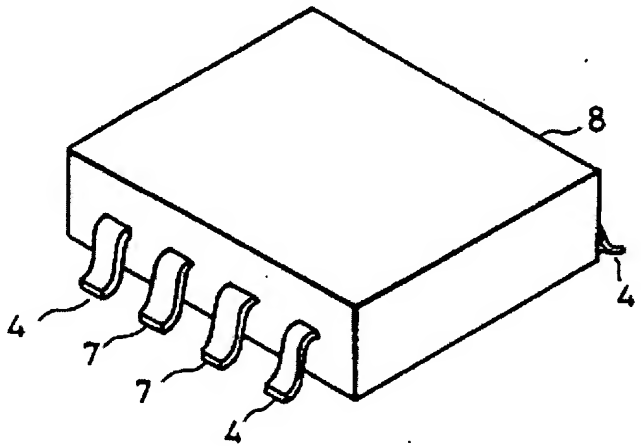


Specifically, the Examiner cited the front and rear ends of die pad (3) receiving bonding wires (5), as comprising the claimed "supplemental downbond diepad portion".

These front and rear end portions of the die pad (3), however, cannot reasonably be understood by the Examiner as teaching explicitly, or even impliedly, the supplemental downbond diepad portion recited by claim 1. In particular, the front and rear ends of die pad (3) are not positioned in the claimed manner between leads that are separate from the diepad. Rather, the ends of the die pad (3) receiving bonding wires (5), are explicitly illustrated as lying between ground leads (4) that are integral with the diepad (3).

Moreover, the claimed "supplemental downbond diepad portion" differs from the front and rear ends of diepad (3) of Figure 2 of the Kadowaki Patent both in terms of structure and function.

Regarding structure, Figure 6 (reproduced above) of the instant application plainly shows "supplemental downbond diepad portion" not extending outside of the package body. This structural characteristic stands in marked contrast with ground leads (7) of the Kadowaki Patent, which in Figure 1 (reproduced below) are shown extending outside the package body to allow electrical contact with the packaged die.



Regarding function, the "supplemental downbond diepad portion" of the package in accordance with embodiments of the present invention, serves to enhance efficiency of utilization of space in the package, freeing up area on the main part of the diepad to support a larger-size die. By contrast, Figure 2 of the Kadowaki patent clearly shows die (1) substantially set back from the edges of the die pad (3) in order to provide space for bonding wires (5) to make contact therewith. Such a configuration serves to reduce the space efficiency of the package, as bonding wires (5) consume space on the main portion of the diepad that could otherwise be occupied by die (1). Such a configuration of the Kadowaki Patent precludes die (1) from having larger dimensions and more fully occupying the available area offered by the die pad.

Based at least upon the failure of the Kadowaki patent to explicitly or even impliedly teach either the structure or function of the present embodiments, it is respectfully asserted that

the claims cannot legitimately be considered anticipated by this reference. These anticipation claim rejections are improper and should be withdrawn.

The Examiner has also rejected claims 6-7 as obvious under 35 U.S.C. 103, based upon the Kadowaki patent in combination with prior art purportedly admitted by Applicants. These obviousness claim rejections are traversed as follows.

The Examiner is respectfully reminded that in order to establish a prima facie case of obviousness, there must be some suggestion or motivation in the references themselves to combine reference teachings, and this teaching or suggestion to make the claimed combination must be found in the prior art, rather than be based upon applicants' disclosure. (Emphasis added; MPEP 2143, citing In re Vaeck, 947 F.2d 488 (Fed. Cir. 1991)).

In the instant case, the Examiner, upon noting the failure of the Kadowaki patent to teach all of the elements of claims 6-7, has turned to Applicants' own disclosure to provide the missing teaching. This argument smacks of hindsight:

> The tendency to resort to "hindsight" based upon applicant's disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art. (Emphasis added; MPEP 2142)

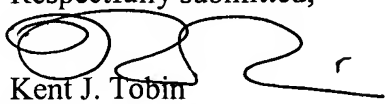
The Kadowaki patent relates to a microwave semiconductor device. This reference contains no teaching, or even suggestion, for its combination with the with a power integrated circuit (IC) package.

Of course, the instant application is replete with suggestion and motivation to employ the techniques disclosed for packaging such power IC die. However, resort by the Examiner to Applicants' own disclosure to provide this motivation or suggestion for combination is strictly prohibited as impermissible hindsight. Such hindsight reasoning cannot be masked in the guise of reliance upon admitted prior art. The instant obviousness rejections are improper and should be withdrawn.

In view of the foregoing, Applicants believe all claims pending in the instant patent Application are now in condition for allowance. Issuance of a formal Notice of Allowance at an early date to this effect is therefore respectfully requested. If the Examiner believes a telephone

conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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